AMENDMENTS TO THE CLAIMS

1. (Previously Presented) A method for erasing a nitride read only memory (NROM) block comprising a plurality of short channel memory cells each having a channel length less than 0.2 microns, a gate input and two source/drain regions, the method comprising:
erasing the memory block; and
performing a recovery operation on the plurality of memory cells such that a threshold voltage indicating a programmed state, for over-erased cells, is increased by coupling the gate input to a ramped voltage, a first source/drain region to a first constant voltage in a range of 3V to 7V, and the remaining source/drain region to a second constant voltage in a range of 0V to 3V.

2. (canceled)

3. (Original) The method of claim 1 wherein the ramped voltage starts in a range of -3 to 0V and ends in a range of 1 to 3V.

4. (Original) The method of claim 3 wherein the ramp voltage has a time period in a range of 10 microseconds to 1 second from start to end.

5 - 6 (canceled)

7. (Original) The method of claim 1 wherein the nitride read only memory cell is embedded in a CMOS device.

8. (currently amended) A method for erasing a nitride read only memory (NROM) block comprising a plurality of short-channel memory cells each having a channel length less than 0.2 microns, a gate input and two source/drain regions, the method comprising:
erasing the memory block; and
performing a recovery operation on the plurality of memory cells such that a threshold voltage indicating a programmed state, for over-erased cells, is increased, the recovery operation includes biasing each of the plurality of memory cells with a ramped voltage on the gate input, a constant voltage in a range of 3V to 7V on a first source/drain region and the remaining source/drain region is ~~left~~ floating.

9. (original) The method of claim 8 and further comprising an oxide-nitride-oxide region, between the first and second source/drain regions, that can hold a single data bit.

10. (currently amended) The method of claim 8 wherein the ~~constant voltage is in a range of 3 to 7V and the~~ ramped voltage starts in a range of -3 to 0V and ends in a range of 1 to 3V over a time period in a range of 10 microseconds to 1 second.

11. (original) The method of claim 8 wherein erasing the memory block includes biasing each of the plurality of cells with a first constant voltage on the gate input, a second constant voltage on a first source/drain region, and a third constant voltage on the remaining source/drain region.

12. (original) The method of claim 11 wherein the first constant voltage is in a range of –12 to 0, the second constant voltage is in a range of 3 to 8V, and the third constant voltage is in a range of 3 to 8V.

13. (original) The method of claim 11 wherein the first source/drain region acts as a drain connection and the remaining source/drain region acts as a source region.

14. (original) The method of claim 13 wherein the source region is allowed to float.

15. – 21. (Canceled)